IN THE SPECIFICATION:

Please amend paragraph [0018], on page 7, as follows:

[0001] Since **CLK** goes low and **CLK'** follows high, the second NMOS transistor (46) and the second PMOS transistor (44) switch 'off,' respectively. Because both the second PMOS transistor (44) and the second ~~PMOS~~ NMOS transistor (46) switch 'off,' the slave transmission gate does not conduct, i.e., the slave transmission gate is 'off,' and the input to the slave stage (34) from the output of the first inverter (40) in the master stage (32) does not pass through the slave transmission gate to the input of the third inverter (48).